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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/720,585	11/24/2003	Erik R. Altman	YOR920030405US1	5059

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EXAMINER	
LAI, VINCENT	

ART UNIT	PAPER NUMBER
2181	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/720,585	ALTMAN ET AL.	
	Examiner	Art Unit	
	Vincent Lai	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6,10,11,14,15,19,20,22-25,27,31,32,35,36,40,41 and 43* is/are rejected.

7)☒ Claim(s) *5,7-9,12,13,16-18,21,26,28-30,33,34,37-39,42 and 44* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on March 29, 2004 was considered by the examiner.

Response to Arguments

2. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

3. Applicant's arguments with respect to claims 1-44 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3, 6, 10, 11, 14, 15, 19, 20, 22-24, 27, 31, 32, 35, 36, 40, 41, and 43 are rejected under 35 U.S.C. 102(b) as being anticipated by Kubota et al (U.S. Patent # 6,308,258 B1), herein referred to as Kubota.

As per **claim 1**, Kubota discloses a digital data processor (See figure 2: Element 30 is the CPU) comprising an instruction unit (See figure 2: Figure 2 highlights the instruction unit of the CPU), said instruction unit comprising a code page that is partitioned for storing in a first section thereof a plurality of instruction words (See column 9, lines 25-26: Instruction register 150) and, in association with at least one instruction word, in a second section thereof an extension to said at least one instruction word (See column 9, lines 29-33: The decoder separates immediates from an instruction and places them in a separate register).

As per **claim 2**, Kubota discloses where said first section is comprised of a first plurality of contiguous storage locations (See figure 2 and column 9, lines 25-26: Instruction register 150 is a contiguous storage location), and where said second section is comprised of a second plurality of contiguous storage locations (See column 9, lines 29-33: Since the instruction register is contiguous, the associated external registers must also be due to their association with the instructions), and where at least one instruction word and said extension to said at least one instruction word are one of fixed length and variable length program instructions (See column 9, lines 25-33 and lines 50-57: Instructions without immediates are normal length while instructions with immediates are longer since the immediate is expanded).

As per **claim 3**, Christie discloses further comprising at least one page table entry bit having a state for indicating, on a code page by code page basis, whether the

code page is partitioned into said first and second sections for storing instruction words and at, least one instruction word extension, or whether the code page is comprised instead of a single section storing only instruction words (See figure 3, and column 10, lines 41-62: A state machine is shown in figure 3 and explained in the specification for situations with immediates).

As per **claim 6**, Kubota discloses further comprising address circuitry for addressing an instruction word in said first section using a current instruction address, while simultaneously addressing an extension to said instruction word at a fixed offset from said current instruction address. (See figure 2 and column 9, lines 25-33 and lines 50-57: When an instruction with an immediate is executed, the immediate data generation circuit 170 will perform functions to ensure that the immediate is available).

As per **claim 10**, Kubota teaches where each instruction word has a width of x bits (See column 8, lines 7-9: This embodiment teaches instructions are 16-bits), where each extension has a width of y bits (See column 8, lines 7-9: This embodiment teaches immediates are 32-bits) where x=n(8-bits) (See column 8, lines 7-9: n would be 2 in this embodiment), where y=m(8-bits), where n is an integer greater than one, and where m has a value less than one, equal to one, or greater than one (See column 8, lines 7-9: m would be 4 in this embodiment).

As per **claim 11**, Kubota discloses further comprising circuitry, coupled to an output of said code page, to combine an addressed instruction word read out of said code page with a corresponding instruction word extension that is also read out of said code page (See figure 2 and column 9, lines 25-33 and lines 50-57: If an instruction requires an immediate, an immediate would be read out).

As per **claim 14**, Kubota discloses where said combining circuitry comprises an input stage of an instruction pipeline (See figure 2: The top portion of the figure shows how an instruction is input).

As per **claim 15**, Kubota discloses where said combining circuitry comprises an instruction decode stage of an instruction pipeline (See figure 2: Instruction decoder circuit 160).

As per **claim 19**, Kubota discloses a digital data processor as in claim 1, where said instructions comprise Reduced Instruction Set Computer (RISC) instructions (See column 7, lines 6-7: RISC architecture is a disclosed embodiment).

As per **claim 20**, Kubota discloses a digital data processor as in claim 19, where said RISC instructions have a width of 32-bits (See column 21, lines 4-13: One of the embodiments has 32-bit instructions), where said at least one extension has a width of 8-bits (See column 19, lines 35-43: An 8-bit immediate is disclosed).

As per **claims 22-24, 27, 31, 32, 35, 36, 40, 41, and 43**, they are rejected for reasons similar to claims 1-3, 6, 10, 11, 14, 15, 19, 20, and 1, respectively. With the exception of claim 43, all the claims are the method used with the digital data processor of the above rejections. Claim 43 is the computer program stored on a computer readable medium of the digital data processor.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 4 and 25 rejected under 35 U.S.C. 103(a) as being unpatentable over Kubota in view of Examiner's use of Official Notice.

As per claim 4, Kubota teaches the digital data processor of claim 3, but does not teach a TLB.

One having ordinary skill in the art would recognize that a TLB would be useful in buffering to ensure that timing is correct.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

A TLB is well known in the art and have been used in the computer processor field prior to the invention of the Applicant. Kubota does not teach TLBs but recognizes a concern for timing, as exhibited by the timing chart in figure 5. One having ordinary skill in the art would recognize the primary use of TLBs are used to speed up certain memory operations such as fetches and thus would be of great use when timing is a concern. Given the wide-use of TLBs in the field of endeavor and the speed up it provides, it would be obvious to one having ordinary skill in the art to have modified the invention taught by Kubota by including a TLB for the purposes of buffering the data and ensuring that correct timing is established.

Allowable Subject Matter

6. Claims 5, 7-9, 12, 13, 16-18, 21, 26, 28-30, 33, 34, 37-39, 42, and 44 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The primary reasons for indicating possible allowance of the limitations of claims 5 and 26 instant application rest at least in the combination of the independent claim with the inclusion of the limitation that "further comprising address fault circuitry for

determining, in accordance with a state of the at least one page table entry bit, whether a generated instruction address is a valid address for the code page." The prior art of record neither anticipates nor renders obvious the above-recited combination.

The primary reasons for indicating possible allowance of the limitations of claims 7 and 28 in the instant application rest at least in the combination of the independent claim with the inclusion of the limitation that "where at least some of the second storage locations are not allocated for storing instruction word extensions." The prior art of record neither anticipates nor renders obvious the above-recited combination.

Because claims 8 and 29 depend directly or indirectly on any of the claims 7 and 28, these claims have limitations which are considered allowable for at least the same reasons noted above with respect to claims 7 and 28.

The primary reasons for indicating possible allowance of the limitations of claims 9, 30, and 44 in the instant application rest at least in the combination of the independent claim with the inclusion of the limitation that "ensuring that a next instruction address is not contained in the second section." The prior art of record neither anticipates nor renders obvious the above-recited combination.

It is noted that claim 44 does not recite the exact limitation of above, but does recite limitations that can be summarized by what is stated above.

The primary reasons for indicating possible allowance of the limitations of claims 12, 13, 33, and 34 in the instant application rest at least in the combination of the independent claim with the inclusion of the limitation that "an instruction cache having a bit width w at least equal to a width of an instruction word plus a width of the instruction word extension." The prior art of record neither anticipates nor renders obvious the above-recited combination.

It is noted that claims 13, and 34 do not recite the exact limitation of above, but does recite limitations that can be summarized by what is stated above.

The primary reasons for indicating possible allowance of the limitations of claims 16 and 37 in the instant application rest at least in the combination of the independent claim with the inclusion of the limitation that "to selectively combine, in response to the state of said *at least one page table entry bit*, an addressed instruction word read out of said code page with a corresponding instruction word extension that is also read out of said code page." The prior art of record neither anticipates nor renders obvious the above-recited combination.

Because claims 17, 18, 38, and 39 depend directly or indirectly on any of the claims 16 and 37, these claims have limitations which are considered allowable for at least the same reasons noted above with respect to claims 16 and 37.

The primary reasons for indicating possible allowance of the limitations of claims 20, and 42 instant application rest at least in the combination of the independent claim

with the inclusion of the limitation that "where said code page has a storage capacity of 4096 bytes, where said first section comprises 3072 bytes, and where said second section comprises 1024 bytes" The prior art of record neither anticipates nor renders obvious the above-recited combination.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents are cited to show further art related to the application:

U.S. Patent # 5,390,307 to Yoshida, directed to instructions composed of instructions and an extension.

U.S. Patent # 5,854,921 to Pickett, directed to registers, which sometimes uses extensions for its instructions.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent Lai whose telephone number is (571) 272-6749. The examiner can normally be reached on M-F 8:00-5:30 (First BiWeek Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vincent Lai
Examiner
Art Unit 2181

vl
June 9, 2007

/DONALD SPARKS/
SUPERVISORY PATENT EXAMINER